Appendix B

NCTA and The NCTA Engineering Committee

The National Cable Television Association (NCTA) has, since 1952, represented the diverse and growing cable industry before Congress and Federal agencies, in courts of law and before state regulatory agencies. As the principal trade association of the U.S. cable television industry, its members comprise cable television system operators, equipment manufacturers, program suppliers and several ancillary service providers.

Members are provided with several forums where they may exchange information on developments in the industry and maintain liaison with other industries, societies and groups. The NCTA Engineering Committee is one such forum. Two-day, bi-monthly meetings held mainly at NCTA's Washington, D.C., headquarters, attract 50 to 60 top-level member and non-member cable engineers from all over the country. Subcommittee chairmen reports form an important segment of each agenda. Participation in subcommittee work and engineering committee meetings are some of this industry's most challenging but rewarding endeavors requiring unusual professional dedication and acumen. Interested, qualified parties should contact the NCTA science and technology department for more details on the meetings. For further information on NCTA membership, call or write:

National Cable Television Association
Association Affairs Department
1724 Massachusetts Ave., N.W.
Washington, D.C. 20036
(202) 775-3550

APPENDIX F: EIA IS-6 STANDARD

AMERICAN NATIONAL STANDARD

ANSI/EIA-563-1990

APPROVED: May 18, 1990

EIA

STANDARD

EIA-563

Standard Baseband (Audio/Video) Interface Between NTSC Television Receiving Devices and Peripheral Devices

EIA-563

AUGUST 1990

ELECTRONIC INDUSTRIES ASSOCIATION

ENGINEERING DEPARTMENT

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STANDARD BASEBAND (AUDIO/VIDEO) INTERFACE BETWEEN NTSC TELEVISION RECEIVING DEVICES AND PERIPHERAL DEVICES

(From EIA Standards Proposal No. 2249, formulated under the cognizance of the R-4 Committee on Television Receivers.)

1.0 BACKGROUND

Television manufacturers have responded to the cable television market by offering models which tune both broadcast and cable only channels. One or more cable channels may be scrambled or encrypted to support a marketing plan, e.g., tiering, premium extra-pay channels, or for security reasons.

These scrambled or encrypted channels may be viewed by a subscriber through the use of a converter/decoder normally provided by a cable system operator. This converter/decoder will tune the full range of cable channels and decode or unscramble as necessary, providing an output to the subscriber's television receiver on a broadcast channel. The subscriber is thus unable to make a full use of remote tuning or other features of the cable-compatible receiver. Additionally, confusion can arise from the need to employ two different remote transmitters to operate both the receiver and the converter/decoder. Also, unnecessary expense results from the duplication of tuning, IF and remote control systems.

One solution to the problem is to provide a baseband interface on the television receiver to accommodate a decoder designed to be compatible with this interface. It is not practicable to provide for all possible interfaces or to accommodate every possible coding scheme. It is believed that the most urgent need will be met if the interface is designed in terms of baseband audio and video signals, together with appropriate control busses. Such signals are relatively standard and, thus, this same interface can be used with other peripheral devices, e.g., video discs, video tape recorders, teletext decoders, DBS or MDS receivers, and future consumer products.

The decoder interface, when used with a cable system, will permit the cable operator to reduce the cost of equipment which he normally provides to the subscriber and, at the same time, enable the subscriber to make full use of the features of a television receiver having the interface.

2.0 SCOPE

This standard defines the interface between a television receiver or VCR designed for the reception of either NTSC (CCIR System M) or cable transmissions with a cable system decoder, or other audio/video device. The interconnections are at baseband (audio and video). The possible configurations of the interface are detailed in Section 6.

3.0 GENERAL REQUIREMENTS

3.1 The interconnecting cable length is normally less than two (2) meters.

3.2 Sync regeneration by a decoder shall conform to the NTSC signal standards as defined in EIA Industrial Electronics Tentative Standard No. 1.

3.3 High or low ac line voltage shall not cause parameters to fall outside the specified ranges.

3.4 Synchronization provided by an external video source may be non-interlaced, but should otherwise be identical to NTSC signal standards.

3.5 Receiver performance specified herein shall be met over the full tuning range.

3.6 The luminance modulation, including data and sync, shall be between 12.5% - 100% at all times.

3.7 The connector specifications are to be found in Appendix C. The connector on the receiver shall be a female connector.

3.8 All peripheral equipment designed in compliance with this standard will normally have a "loopthru" 20 pin and shield connector, in addition to and identical in function to the original interface connector. All lines not simply wired through are to be buffered to attain the correct impedance and level at the second connector.

3.9 When operating with scrambling systems which do not derive audio from the sound carrier the receiver may not quiet the sound channel during acquisition unless a sound carrier is present.

3.10 The receiver should be designed in such a way as to withstand, in the "off" state, signals and terminations permitted in the "on" state. In addition, the receiver shall, when in the "off" state, provide no termination of a lesser impedance than that specified in the "on" state. It is assumed that in the "off" state the receiver shall provide some impedance to ground at each pin, possibly excepting the control lines, some or all of which may behave as though the receiver were on.

3.11 It is expected that video will always be present at Pin 19 of the receiving device, except during channel changing, even though the video is not being processed by the peripheral device.

3.12 A ground must always be provided on Pin 13 (FB/Chroma Gnd) of the receiving device even though the options are not implemented.

4.0 RECEIVER INTERFACE DEFINITIONS

NOTE: Definitions of control logic, as used in this standard, are to be found in Appendix A.

4.1 Pin 1 - Audio Select Function (open collector logic)

This function permits the peripheral device to control the audio source of the receiver as follows:

OPTION	LEVEL
Internal Audio	High
External Audio (Pins 2 & 6)	Low

4.2 Pin 2 - Audio Input, Left Channel

4.2.1 - Amplitude at Equivalent of 100% Modulation shall be 400 mV RMS $\pm$ 150 mV RMS

4.2.2 - Input Impedance $\geq$ 10k ohms

4.3 Pin 3 - AGC Time Constant/Video Select Function (open collector logic)

Pin 3 works in conjunction with Pin 18 to select either the AGC time constant or the video source, as indicated in the following table:

Pin 3	Pin 18	AGC	Video Source
1	1	normal	internal
0	1	normal	external
1	0	fast	external
0	0	slow	external

NOTE: The receiver is to be designed with a slow and fast mode of AGC operation. In the "fast" AGC mode the receiver AGC time constant requirements are:

- o $\leq$ 1 ms for 6 dB increase (RF increment)
- o $\leq$ 2 ms for 6 dB decrease (RF decrement)
- o Test steps will be 0 - 6 dBmV and 6 - 0 dBmV
- o Tests will be made at 0 and 100 IRE unit flat fields
- o Test level change shall not occur during the vertical interval

NOTE: In the receiver "slow" AGC mode the time constant requirements are $\geq$ 20 ms tested as above.

4.3.1 The transient change in peak-to-peak video at Pin 19, in response to a change between any two time constant states, shall be <10%. This applies for times greater than 100 ms after a channel change with <12 dB RF level change.

4.4 Pin 4 - Audio Ground for Pins 2, 6 and 8.

4.5 Pin 5 - Second Audio Program (SAP) Select Function

This pin is used to indicate to the peripheral device that the SAP channel is to be selected.

OPTION	LEVEL
SAP Audio	low
Normal Audio	high

4.6 Pin 6 - Audio Input, Right Channel

(See Section 4.2 for parameters.)

4.7 Pin 7 - B-Y Channel (complies with ANSI T14.31-339)

4.7.1 DC Level not to exceed ±1.0 volt into 75 ohms.

4.7.2 Input Termination 75 ohms ± 5% to ground. Coupling beyond the input terminating resistor may be ac or direct-coupling.

4.7.3 Horizontal blanking must be present.

4.8 Pin 8 - Wideband Audio Output

4.8.1 Amplitude (into 10k ohms ± 1%) 1.2 V ± 3%

NOTE: Signal as in Section 4.19.1, with aural carrier deviation ± 75 kHz at 300 Hz

4.8.2 Output Impedance: 600 ohm ± 10%

4.8.3 Frequency Response: -3 dB point with respect to 300 Hz shall be > 90 kHz

4.8.3.1 Amplitude ripple with respect to 300 Hz over the range of 50 Hz to 47 kHz should be less than ± 0.35 dB

4.8.3.2 Phase response from linear over the range of 50 Hz to 47 kHz should be less than ± 3 degrees

4.8.4 Noise and Distortion

NOTE: All levels are with respect to a 25 kHz deviation (300 Hz rate) signal.

4.8.4.1 Thermal Noise: <-62 dB for a bandwidth of 15 kHz (no de-emphasis). Measured with no video modulation.

4.8.4.2 Buzz: <-50 dB for a bandwidth of 15 kHz. Video is a 100 IRE unit Flat Field.

4.8.4.3 Horizontal Components:

Harmonic of fH	Limit (dB)
1,2,3	<-30
4,5,6	<-37

Video is a 100 IRE unit Flat Field.

4.8.4.4 Distortion: <2% THD for 70 kHz deviation at a 1 kHz rate. Measured with no video modulation (Does not include horizontal components.)

4.9 Pin 9 - Video Format - This Pin is used in conjunction with Pin 20 to indicate the video format to the receiver as follows:

Video Format	Pin 9	Pin 20
composite video	1	1
Y/R-Y/B-Y	0	0
Y/C	1	0

NOTE: Pin 9 conforms to open collector logic (1=open)
Pin 20 logic: 0 = 0.0 < V < 0.4 (into 75 ohm to gnd)
1 = 0.4 < V < 3.0 (into 75 ohm to gnd)
(Video present as per 5.20)

4.10 Pin 10 - Communication to Peripheral

This pin is used to provide unidirectional communication from the receiver to peripheral(s). Logic levels are given by the receiver control line logic convention in Appendix A. Communication coding and protocols are to be found in Appendix B.

4.11 Pin 11 - Luminance (Y) Input: 1.0 V sync tip to 100 IRE Negative sync, 75 ohms to gnd.

4.12 Pin 12 - Reserved for Future Application (No Connection)

4.13 Pin 13 - Fast Blanking/Chroma Ground (This Pin will always be grounded at the receiver)

4.14 Pin 14 - Channel Change and Power Indicator Function

This pin is used to indicate to a decoder when a channel change is in process and also the state of the receiver power. The decoder may sense the duration of signal dwell in the low state to identify channel change or receiver power off.

RCVR STATE	LEVEL
Power On	high
Channel Change in process	low for $\geq$ 5 ms and $\leq$ 2.0 s
Power Off	low for > 2.0 s

4.15 Pin 15 - R-Y Channel (complies with ANSI T14.31-339)

(See Section 4.7 for parameters.)

4.16 Pin 16 - Fast Blanking Function/Chroma Input

4.16.1 Blanking Logic Levels (into 75 ohms to ground)

Low (internal video): 0.0 V to 1.2 V
High (external): 1.8 V to 3.0 V

4.16.2 Rise/Fall Time

> 40 ns into 75 ohm load measured from maximum low level to minimum high level

4.16.3 Output Impedance/Drive Capability: 75 ohm $\pm$ 5% capable of driving a 75 ohm load

4.16.4 Chroma Signal: 3.58 MHz burst, 0.286 V p-p
75 ohm ac coupled

4.17 Pin 17 - Video, Y, R-Y, and B-Y Ground

4.18 Pin 18 - Decoder Present Function and Decoder Restored Sync (DRS) (for AGC)

4.18.1 Impedance

Shall be 2k ohm $\pm$ 5% (tied to 5.0 V $\pm$ 0.5 V)

4.18.2 Sync Amplitude

The sync tip shall be the most negative part of the DRS signal by ≥ 200 mV (excluding chrominance).

4.18.3 Sync Tip Level

Shall be within 0.05 V of sync level presented to the decoder at Pin 19.

NOTE: The sync tip level of the decoder restored sync must vary in proportion to the receiver second detector output (i.e., video output Section 4.19) so as to be useful in driving the receiver AGC generator. When properly authorized, the decoder must restore a scrambled signal so that the sync tip level of output (Section 5.18)/input (Section 4.18) does not change between scrambled and unscrambled operation. Whenever proper receiver AGC is needed this signal must contain composite sync and may be a full composite video signal.

NOTE: The decoder restored sync output, measured relative to zero carrier level (2.14 V) is intended to be a replica of the sync that would be present if the signal were not scrambled. The decoder must therefore measure a recurring parameter(s) in the video from the receiver and cause the decoder restored sync to be nominal when the parameter is nominal, proportionally smaller than nominal when the parameter is smaller than nominal, and proportionally larger when the parameter is larger.

Suitable positive scale factor is to be chosen by the decoder design which will result in the sync pulse tip being equal to its scale factor times the recurring parameter amplitude. Decoder shall increase the sync tip output level relative to zero carrier in order to decrease the receiver's gain.

4.18.4 Logic Levels

This pin is used to indicate to a receiver when DRS is active and decoder is present. (See following:)

STATE	LEVEL
DRS active, decoder present	0 V to 3.0 V
DRS off, decoder not present	4.0 V to 5.5 V

NOTE: Decoder is only required to provide a dynamic range of 0.5 V to 1.35 V sync tip level DRS for AGC control.

4.19 Pin 19 - Receiver Video Output when terminated into 75 ohms to ground (from Antenna Input to Output to peripheral Device)

NOTE: The receiver video at Pin 19 shall reach steady state within 0.5 s of Pin 18 switching to the DRS active state.

4.19.1 Amplitude Response

Frequency	Amplitude
0.5 MHz	0 dB ± 2 dB
1.0 MHz	0 dB ± 0 dB
2.0 Mhz	0 dB ± 2 dB
3.0 MHz	0 dB +2 dB -4 dB
3.58MHz	0 dB +2 dB -6 dB
4.2 MHz	not specified
4.5 MHz	<-40 dB

NOTE: Data for Section 4.19.1 shall be taken with the input signal per NTC Report No. 7, Section 3.8, modulated to 75% with standard envelope delay predistortion and with an aural carrier 15 dB below the visual carrier.

NOTE: The 4.5 MHz measurement requires a separate test. Normally 4.5 MHz will not be present in the receiver output.

4.19.2 Chrominance - Luminance Delay Inequality <150 ns

NOTE: Data for Section 4.19.2 shall be taken with the input signal per NTC Report No. 7, Section 3.7, modulated to 75% with standard envelope delay predistortion.

4.19.3 Differential Phase <5 degrees

NOTE: Data for Section 4.19.3 shall be taken with the input signal per NTC Report No. 7, Section 3.14, modulated to 87.5%.

4.19.4 Differential Gain <10%

NOTE: Data for Section 4.19.4 shall be taken with the input signal per NTC Report No. 7, Section 3.13,modulated to 87.5%.

NOTE: Sections 4.19.3 and 4.19.4 are intended to support video inversion scrambling.

4.19.5 Luminance NonLinear Distortion ≤ 10 IRE units

(Measured at 10%, 50% and 90% APL as per NTC Report No.7, Section 3.9.)

4.19.6 Preshoot or Overshoot Amplitude ≤ 10%

(0-100 IRE unit luminance transition of the video signal with proper envelope delay distortion, 2T bar risetime and 75% modulation)

4.19.7 Absolute Value of Difference Between Percentage Overshoot and Percentage Overshoot
= [% Preshoot - % Overshoot] ≤ 5%
(Use the same test condition as Section 4.19.6.)

4.19.8 Video Amplitude

Blanking to Peak White 0.71 V ± 0.10 V

Sync tip to Blanking 0.29 V ± 0.06 V

4.19.9 Sync Polarity Negative

4.19.10 Output Impedance 75 ohm ± 5% (Direct-coupled)

4.19.11 DC Level at 100 IRE units 2.00 V ± 0.10 V

4.19.12 The instantaneous video level shall be confined between ±3.0 volts.

4.19.13 Minimum Dynamic Range 0.50 V to 2.14 V

NOTE: This benefits acquisition where gain is most likely high, and could result in excessive distortion (particularly by noise inverters).

4.20 Pin 20 - Receiver Video Input

4.20.1 Video Amplitude Accepted (Sync tip to peak white) 1.00 V ± 0.25 V

4.20.2 Sync Polarity Accepted Negative

4.20.3 Input Termination 75 ohm ± 5% to ground
(Coupling beyond the input terminating resistor may be ac or direct-coupling.)

4.20.4 Return Loss (3.58 MHz relative to 75 ohm) ≥ 20 dB

4.20.5 When a peripheral device is connected, receiver synchronization shall be controlled via Pin 20.

4.20.6 The receiver must tolerate ±3.0 volts.

5.0 PERIPHERAL DEVICE INTERFACE DEFINITIONS

NOTE: Definitions of control logic, as used in this standard, are to be found in Appendix A.

5.1 Pin 1 - Audio Select Function (open collector logic)

This function permits the peripheral device to control the audio source for the receiver as follows:

OPTION	LEVEL
Internal Audio	High
External Audio (Pins 2 & 6)	Low

5.2 Pin 2 - Audio Output, Left Channel

NOTE: The peripheral device may be required to drive a load consisting of Pins 2 and 6 connected together inside the receiver via impedances of not less than 10k ohm to permit the use of a stereo peripheral device with a mono receiver. (See Figure 1)

5.2.1 - Amplitude at Equivalent of 100% Modulation shall be 400 mV RMS ± 150 mV RMS into 10k ohm load.

5.2.2 - Output Impedance < 1k ohm

5.3 Pin 3 - AGC Time Constant/Video Select Function (open collector logic)

Pin 3 works in conjunction with Pin 18 to select either the AGC time constant or the video source, as indicated in the following table:

Pin 3	Pin 18	AGC	Video Source
1	1	normal	internal
0	1	normal	external
1	0	fast	external
0	0	slow	external

NOTE: When the receiver is tuned to a non-encoded NTSC signal, a decoder shall place the receiver in the normal AGC mode within 5 seconds.

5.3.1 The transient change in peak-to-peak video at Pin 19, in response to a change between any two time constant states, shall be <10%.

5.4 Pin 4 - Audio Ground for Pins 2, 6, and 8.

5.5 Pin 5 - Second Audio Program (SAP) Select Function

This pin is used by the receiver to indicate to the peripheral device that the SAP channel is to be selected as the audio source to the receiver.

OPTION	LEVEL
SAP Audio	low
Normal Audio	high

5.6 Pin 6 - Audio Output, Right Channel

See Section 5.2 for parameters.

5.7 Pin 7 - B-Y Channel (complies with ANSI T14.31-339)

5.7.1 DC Level not to exceed ±1.0 volt into 75 ohms.

5.7.2 Input Termination 75 ohms ± 5% to ground. Coupling beyond the input terminating resistor may be ac or direct-coupling.

5.7.3 Horizontal blanking must be present.

5.8 Pin 8 - Wideband Audio Input
5.8.1 Amplitude (into 10k ohms ± 1%) 1.2 V ± 3%

5.8.2 Input Impedance (ac coupled) ≥10k ohm

5.8.3 Frequency Response: -3 dB point with respect to 300 Hz shall be > 50 kHz

5.8.3.1 Amplitude ripple with respect to 300 Hz over the range of 50 Hz to 47 kHz shall be ± 0.35 dB

5.8.3.2 Phase response from linear over the range of 50 Hz to 47 kHz shall be ± 3 degrees

5.8.4 Noise and Distortion

NOTE: All levels are with respect to a 25 kHz deviation (300 Hz rate) signal.

5.8.4.1 Thermal Noise: <-62 dB for a bandwidth of 15 kHz (no de-emphasis). Measured with no video modulation.

5.8.4.2 Buzz: <-50 dB for a bandwidth of 15 kHz. Video is a 100 IRE unit Flat Field.

5.8.4.3 Horizontal Components:

Harmonic of $f_{(H)}$	Limit (dB)
1,2,3	<-30
4,5,6	<-37

Video is a 100 IRE unit Flat Field.

5.8.4.4 Distortion: <2% THD for 70 kHz deviation at a 1 kHz rate. Measured with no video modulation. (Does not include horizontal components.)

5.9 Pin 9 - Video Format - This pin is used in conjunction with Pin 20 to indicate the video format to the receiver as follows:

Video Format	Pin 9	Pin 20
composite video	1	1
Y/R-Y/B-Y	0	0
Y/C	1	0

NOTE: Pin 9 conforms to open collector logic (1=open) Pin 20 logic:
0 = 0.0 < V < 0.4 (into 75 ohm to gnd)
1 = 0.4 < V < 3.0 (into 75 ohm to gnd)
(video present as per 5.20)

5.10 Pin 10 - Communication from Receiver

This pin is used to provide unidirectional communication from the receiver to peripheral(s). Logic levels are given by the receiver control line logic convention in Appendix A. Communication coding and protocols are found in Appendix B.

5.11 Pin 11 - Luminance (Y) Output: 1.0 V ± 20% sync tip to 100 IRE, Negative sync, into 75 ohms to ground.

5.12 Pin 12 - Reserved for Future Application (No Connection)

5.13 Pin 13 - Fast Blanking/Chroma Ground
(This pin will always be grounded at the receiver)

5.14 Pin 14 - Channel Change and Power Indicator Function

This pin is used to indicate to a decoder when a channel change is in process and also the state of the receiver power. The decoder may sense the duration of signal dwell in the low state to identify channel change or receiver power off.

RECEIVER STATE	LEVEL
Power On	high
Channel Change in process	low for ≥ 5 ms and ≤ 2.0 s
Power Off	low for > 2.0 s

5.15 Pin 15 - R-Y Channel (complies with ANSI T14.31-339)

See Section 5.7 for parameters.

5.16 Pin 16 - Fast Blanking Function/Chroma Output

5.16.1 Blanking Logic Levels (into 75 ohms to ground)

Low (internal video): 0.0 V to 1.2 V
High (external): 1.8 V to 3.0 V

5.16.2 Rise/Fall Time

> 40 ns into 75 ohm load measured from maximum low level to minimum high level

5.16.3 Output Impedance/Drive Capability: 75 ohm ± 5%
capable of driving a 75 ohm load

5.16.4 Chroma Signal. 3.58 MHz burst, 0.286 V p-p

5.17 Pin 17 - Video, Y, R-Y, and B-Y Ground

5.18 Pin 18 - Decoder Present Function and Decoder Restored Sync (for AGC)

5.18.1 Load Impedance at Receiver

Shall be 2k ohm ± 5% (tied to 5.0 V ± 0.5 V)

5.18.2 Sync Amplitude

The sync tip shall be the most negative part of the DRS signal by ≥ 200 mV (excluding chrominance).

5.18.3 Sync Tip Level

Shall be within 0.05 V of the sync level extrapolated to that of an equivalent nonscrambled signal presented at Pin 19

NOTE: Decoder Restored Sync (DRS) allows the decoder to control the receiver's AGC system. (In the active state) this signal must contain composite sync, and may be a full composite video signal. DRS is intended to provide a replica of nonscrambled sync for the purposes of AGC. The DRS sync timing shall be coincident with the sync at Pin 20.

An expression describing the sync tip voltage with respect receiver gain is as follows:

$$\text{DRS Sync Tip Voltage} = Vo-(Vo-Vs)/Am = 2.14 - 1.14/Am$$

where Vo = nominal zero carrier voltage (2.14 V)
Vs = the nominal sync tip voltage (1.0 V)
Am = desired (linear) gain.

The sync tip level of DRS must vary in the same manner as nonscrambled video sync would vary for a particular receiver gain. The decoder must therefore measure a recurring parameter(s) in the video from the receiver and cause the decoder restored sync to be nominal when the parameter is nominal, proportionally smaller than nominal when the parameter is smaller than nominal, and proportionally larger when the parameter is larger.

In addition to responding to DRS, receiver video amplitude may be subject to variations due to RF level changes, Average Picture Level (APL), nonsuppressed sync, etc. To maintain correct video amplitude and assure system stability, DRS must be updated in accordance with Section 5.18.4.

Suitable positive scale factor is to be chosen by the decoder design which will result in the sync pulse tip being equal to its scale factor times the recurring parameter amplitude. Decoder shall increase the sync tip output level relative to zero carrier in order to decrease the receiver's gain.

5.18.4 DRS Open Loop Response Time

Decoder response time to changes at Pin 19 (to be measured from the the application of a 1 dB step change in composite video at Pin 19 to the 90% settling point at Pin 18) shall be $\leq$ 1.0 ms.

NOTE: The sync tip level of the decoder restored sync must vary in proportion to the receiver second detector output (i.e., video output Section 4.19) so as to be useful in driving the receiver AGC generator. When properly authorized, the decoder must restore a scrambled signal so that the sync tip level of output (Section 5.18)/input (Section 4.18) does not change between scrambled and unscrambled operation. Whenever proper receiver AGC is needed this signal must contain composite sync and may be a full composite video signal.

5.18.5 Decoder Acquisition Time after Authorization < 5 s

This is the maximum time from signal input until return of correct sync to the receiver.

5.18.6 Decoder Transparency

Upon notification of a channel change command, a decoder shall transparently connect Pin 19 to Pin 18 and retain same throughout the acquisition time. If the signal is to be decoded or otherwise monitored then the decoder shall provide Decoder Restored Sync (DRS) on Pin 18, otherwise it shall drive Pin 18 high.

5.18.7 Logic Levels

This pin is used to indicate to a receiver when DRS is active and a decoder is present as follows:

STATE	LEVEL
DRS active, decoder present	0 V to 3.0 V
DRS off, decoder not present	4.0 V to 5.5 V

5.18.8 DRS Dynamic Range 0.5 V to 1.35 V (min range)

NOTE: This benefits acquisition where gain is most likely high, and would result in excessive distortion (particularly by noise inverters).

5.19 Pin 19 - Peripheral Video Input (from Receiver)

5.19.1 Input Termination 75 ohm ± 5% to ground

5.19.2 Return loss at 3.58 MHz relative to 75 ohm ≥ 20 dB

NOTE: Receiver video at Pin 19 may not be present for a maximum of 0.5 s following Pin 18 being switched to the DRS active state.

5.20 Pin 20 - Peripheral Video Output

5.20.1 Video Amplitude (Sync tip to peak white) 1.00 V ± 0.25 V

5.20.2 Sync Polarity Negative

5.20.3 Input Termination at Receiver 75 ohm ± 5% to ground Coupling beyond the input terminating resistor may be ac or direct-coupling.

5.20.4 Decoder Video Gain 1.0 ± 0.1

5.20.5 Decoder Sync Compression ≤ 30%

From Pin 19 to Pin 20, tested with video input of 1.5 V sync tip to peak white

5.20.6 Decoder Video Frequency Response

Frequency	Amplitude
0.5 MHz	0 dB ± 2 dB
1.0 MHz	0 dB ± 0 dB
2.0 Mhz	0 dB ± 2 dB
3.0 MHz	0 dB ± 2 dB
3.58MHz	0 dB ± 2 dB
4.2 MHz	0 dB ± 2 dB

NOTE: Data for Section 5.20.6 shall be taken using the multiburst signal per NTC Report No. 7, Section 3.8

5.20.7 Chrominance - Luminance Delay Inequality ±20 ns

NOTE: Data for Section 5.20.7 shall be taken with the input signal per NTC Report No. 7, Section 3.7, modulated to 75% with standard envelope delay predistortion.

5.20.8 Decoder Differential Phase ± 3 degrees

NOTE: Data for Section 5.20.8 shall be taken with the input signal per NTC Report No. 7, Section 3.14, modulated to 87.5%.

5.20.9 Decoder Differential Gain ± 3%

NOTE: Data for Section 5.20.9 shall be taken with the input signal per NTC Report No. 7, section 3.13, modulated to 87.5%.

NOTE: Sections 5.20.8 and 5.20.9 are intended to support video inversion scrambling keyed to fade to black.

5.20.10 Decoder design is expected to stabilize the back porch of the sync interval to permit the receiver to clamp on the back porch to generate a stable black level.

5.20.11 The instantaneous video level shall be confined between ± 3.0 volts.

5.20.12 Sync regeneration by a decoder shall conform to the NTSC signal standards as defined in EIA Industrial Electronics Tentative Standard No. 1.

6.0 INTERFACE OPTIONS

6.1 This standard allows for two possible interfaces. The particular interface included in an equipment is to be conspicuously marked near the plug. The possible interfaces and corresponding receiver markings are:

OPTION	LABEL
NTSC	EIA - 563
NTSC + Y/C + Color Difference	EIA - 563 - Y/C

NOTE: Regardless of the receiver option, the receiver must function with either a monophonic or stereo decoder or peripheral device. (See Figure 1)

NOTES ON FIGURE 1

(A) MONOPHONIC RECEIVER. A receiver with a monophonic audio amplifier. It may or may not have a built-in decoder for the BTSC System stereo or second audio (SA) program transmissions. It may or may not provide the SA program enable signal. See Note D.

(B) STEREOPHONIC RECEIVER. A TV receiver with stereophonic audio amplifiers and a built-in decoder for BTSC transmissions.

(C) MONOPHONIC DECODER. A cable decoder which unscrambles scrambled video signals. If the cable system scrambles audio, it also descrambles the audio. If the cable system uses a proprietary system of combined audio scrambling and SA encoding, the decoder also decodes the SA program. In the later case, the decoder has a manual override switch so the subscriber can switch to SA program in case the receiver does not have the SA program enable feature. See Note D.

(D) SECOND AUDIO (SA) PROGRAM ENABLE SIGNAL. When the user selects SA program at the receiver, or at its remote control, the receiver pulls Pin 5 low. Decoders which decode cable proprietary SA programs, switch automatically to SA program mode when this signal is received. Receivers may or may not have this feature.

(E) STEREOPHONIC DECODER. A cable decoder which unscrambles scrambled video signals, and also decodes stereo and SA program which are encoded by a cable proprietary system of combined scrambling and stereo/SA program encoding. The decoder has a manual override switch so the subscriber can switch to SA program in case the receiver does not have the SA program enable feature. See Note D.

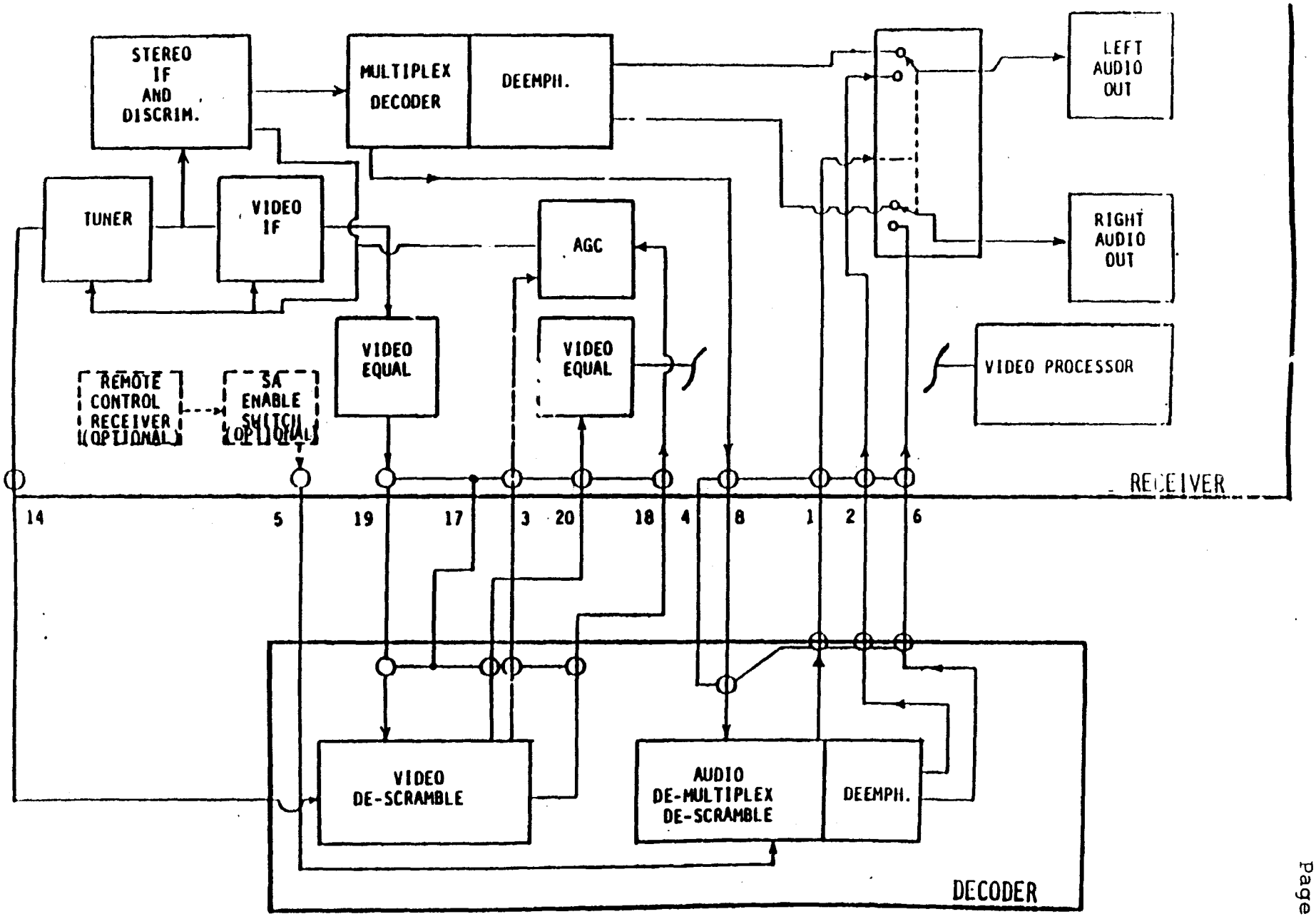


Figure 1

- See Notes

APPENDIX A

Logic Levels

The purpose of this appendix is to define what is meant by TTL and open collector logic for the purposes of the interface control lines and data communication lines in this Standard.

Open collector generally provides pull-up only in the receiver, thus ensuring a high state when open and allowing any number of parallel input devices to force a low state. Except for the breakdown voltage of a driver stage, the choice of receiver pull-up voltage and thus logic level can be made independent of driver specifications. Open collector logic was selected for all receiver inputs to support "daisy chaining", to assure the proper open state, and for consistency.

The logic selected for all receiver outputs is the most cost effective (with no loss in flexibility) and utilizes lower current levels than conventional TTL.

Receiver control line standard: (Pins 5,10,14)

Low Level Output Voltage:	1.0 V Max @ +100 uA
Low Level Input Current:	-30 uA @ 1.0 V
High Level Output Voltage:	4.0 V Min @ -100 uA
High Level Input Current:	+30 uA Max @ 4.0 V

These specifications will support:

- o the use of 1k ohm electrostatic discharge protection,
- o the use of ±10% logic supplies for receiver and peripherals,
- o a fan-out of three,
- o compatibility with CMOS and NMOS devices.

Open collector standard: (Pins 1,3,9)

Low Level Output Voltage:	0.4 V Max
Low Level Output Sinking Capability:	5.0 mA
High Level Output Leakage Current:	25 uA
Input Pull-up Voltage:	7.0 V Max

APPENDIX B

Data Communications Format

The following describes the modulation scheme and coding to be used by the receiver to communicate, via Pin 10, with a peripheral device to support pay-per-view functions. This can be expanded at a later date, if necessary, to support communications for other purposes. The logic levels are described in Appendix A.

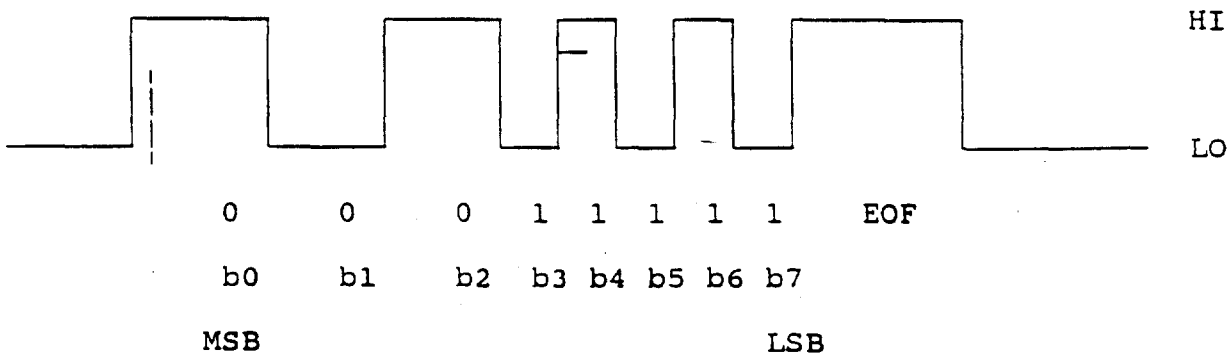
TRANSMISSION SPEED: 1,000 one bits per second

MODULATION TECHNIQUE: Pulse width coding

MESSAGE LENGTH: 8 bits plus end-of-field

TIMING (MICROSECONDS): Pulse width One bit 1,000 ± 100
Pulse width Zero bit 2,000 ± 200
Pulse width End-of-Field 3,000 ± 300

The first 4-bits of the transmission is always **0 0 0 1** which indicates a pay-per-view function/command. The second 4-bits are the actual data/command to be acted upon. The End-Of-Field pulse (high for 3,000 microseconds) marks the end of the last bit (b7). This format can be implemented with a 4-bit microprocessor.



"START: Message, Most Significant Bit **MSB** transmitted first

FIGURE B-1